STIC Search Report
EIC 2100

USPTO

STIC Database Tracking Number: 207758

TO:	From:
Jason Mitchell Location: RND 5B11 Art Unit: 2193 Wednesday, November 29, 2006 Case Serial Number: 10/645269	Byron T. Mims Location: EIC 2100 RND-4B19 Phone: 272-3528 byron.mims@uspto.gov

Search Notes

Jason

Enclosed are art findings that may be of interest. I have tagged as well as highlighted the enclosed retrieved items, which seemed most relevant. Let me know if there is anything in particular that you would like for me to pursue further.

Byron

sira
Search and Information Resources Administration

Green, Shirelle 207758

From: JASON MITCHELL [jason.mitchell@uspto.gov]
Sent: Friday, November 17, 2006 12:25 PM
To: STIC-EIC2100
Subject: Database Search Request, Serial Number: 10/645269

75

Requester:
JASON MITCHELL (P/2193)
Art Unit:
GROUP ART UNIT 2193
Employee Number:
80392
Office Location:
RND 05B11
Phone Number:
(571)272-3728
Mailbox Number:

Case serial number:
10/645269
Class / Subclass(es):
717/114-119
Earliest Priority Filing Date:
8/21/03
Format preferred for results:
Paper

RECEIVED
NOV 17 2006
BY:

Search Topic Information:

I am looking for a "Hardware Description Lanugage / HDL" that provides "syncronization / timing" controls which specify a "pipe / wire / buffer / thread / channel" and a "size / number" of the data written to the "pipe / wire / buffer / thread / channel"

Example formats would be
notify (outpipeName, numberOfElementsWritten)
relese (inpipeName, numberOfElementsRead)

the pipe etc. may be defined as a "data consumer/producer"
Example HDLs are Verilog, VHDL, SpecC

```
Set     Items   Description
S1       3000   HARDWARE(2N)DESCRI?(2N)LANGUAG? OR HDL
S2        399   VERILOG? ? OR VHDL? ? OR SPECC? ? OR VHSIC? ?
S3    6789705   TIME? ? OR TIMING? OR TEMPORAL? OR CLOCK? OR DURATION? OR -
            EVENT? OR SCHEDUL? OR OCCASION? OR DAY? ? OR HOUR? ? OR MINUT-
            E? ? OR SECOND? ? OR PERIOD? OR CHRONOLOG?
S4    1463812   SIMULTANEOUS? OR SYNCHRON? OR COINCID? OR COEXIST? OR CONC-
            URR? OR COORDINAT? OR SAME(2N)TIME? ?
S5    1095852   S3:S4(7N)(SWITCH? OR IMPLEMENT? OR REGULAT? OR CONTROL? OR
            SUBSTITUT? OR RELAY? OR REDIRECT? OR REVERS? OR SHIFT? OR DIV-
            ERT? OR REROUT? OR SHUNT? OR ACTUAT? OR TRIGGER?)
S6    2271030   PIPE? ? OR WIRE? ? OR BUFFER? OR THREAD?
S7     158562   S6(7N)(SELECT? OR BASE? ? OR PICK??? OR CHOOSE? OR DETERMI-
            N? OR CHOSEN OR IDENTIFY? OR IDENTIFIES OR SPECIF? OR DESIGNA-
            T? OR INDICAT? OR DESIR???)
S8          4   S1:S2 AND S5 AND S7
S9         35   S1:S2 AND S7
S10    122961   (WRITE? ? OR WRITING? OR WRITTEN?)(3N)(DATA OR INFO OR INF-
            ORMATION??)
S11      6188   S10(7N)(SIZE? ? OR AMOUNT? OR QUANTIT? OR NUMBER?)
S12      1180   S11(7N)(SELECT? OR BASE? ? OR PICK??? OR CHOOSE? OR DETERM-
            IN? OR CHOSEN OR IDENTIFY? OR IDENTIFIES OR SPECIF? OR DESIGN-
            AT? OR INDICAT? OR DESIR???)
S13         0   S9 AND S12
S14        77   S7 AND S12
S15         0   S14 AND S1:S2
S16        14   S14 AND S5
S17        14   S16 NOT S8:S9
S18         0   S1:S2 AND S12
S19       283   AU=(STEVENS C? OR STEVENS, C?)
S20         0   CAMERON(2N)STEVENS
S21         0   S1:S2 AND S19
File 350:Derwent WPIX 1963-2006/UD=200674
         (c) 2006 The Thomson Corporation
File 347:JAPIO Dec 1976-2006/Jul(Updated 061116)
         (c) 2006 JPO & JAPIO
```

```
Set      Items   Description
S1        7693   HARDWARE(2N)DESCRI?(2N)LANGUAG? OR HDL
S2        1738   VERILOG? ? OR VHDL? ? OR SPECC? ? OR VHSIC? ?
S3     1983074   TIME? ? OR TIMING? OR TEMPORAL? OR CLOCK? OR DURATION? OR -
             EVENT? OR SCHEDUL? OR OCCASION? OR DAY? ? OR HOUR? ? OR MINUT-
             E? ? OR SECOND? ? OR PERIOD? OR CHRONOLOG?
S4      932270   SIMULTANEOUS? OR SYNCHRON? OR COINCID? OR COEXIST? OR CONC-
             URR? OR COORDINAT? OR SAME(2N)TIME? ?
S5      625004   S3:S4(7N)(SWITCH? OR IMPLEMENT? OR REGULAT? OR CONTROL? OR
             SUBSTITUT? OR RELAY? OR REDIRECT? OR REVERS? OR SHIFT? OR DIV-
             ERT? OR REROUT? OR SHUNT? OR ACTUAT? OR TRIGGER?)
S6     1024062   PIPE? ? OR WIRE? ? OR BUFFER? OR THREAD? OR CHANNEL???
S7      245315   S6(7N)(SELECT? OR BASE? ? OR PICK??? OR CHOOSE? OR DETERMI-
             N? OR CHOSEN OR IDENTIFY? OR IDENTIFIES OR SPECIF? OR DESIGNA-
             T? OR INDICAT? OR DESIR???)
S8      150776   S6(7N)(SIZE? ? OR NUMBER? OR QUANTIT? OR AMOUNT?)
S9           0   NOTIF?()(OUTPIPE? OR OUT()PIPE)()NAME? ?
S10          1   NUMBER?(1W)ELEMENT?()WRITTEN
S11          0   RELEASE()INPIPE?()NAME? ?
S12          2   NUMBER?(1W)ELEMENT?()READ
S13         10   S1:S2(100N)S5(100N)S7(100N)S8
S14         41   S1:S2(100N)S5(100N)S7
S15         33   S14 NOT S13
S16         19   S15 NOT (AD>2003 OR AD=2004:2006)
S17        123   AU=(STEVENS C? OR STEVENS, C?)
S18          0   CAMERON(2N)STEVENS
S19          0   S17 AND S1:S2
S20          0   S17(100N)S1:S2
S21          0   S1:S2(100N)S9:S12
File 348:EUROPEAN PATENTS 1978-2006/ 200646
         (c) 2006 European Patent Office
File 349:PCT FULLTEXT 1979-2006/UB=20061123UT=20061116
         (c) 2006 WIPO/Thomson
```

```
Set     Items   Description
S1       3000   HARDWARE(2N)DESCRI?(2N)LANGUAG? OR HDL
S2        399   VERILOG? ? OR VHDL? ? OR SPECC? ? OR VHSIC? ?
S3    6789705   TIME? ? OR TIMING? OR TEMPORAL? OR CLOCK? OR DURATION?
OR -
               EVENT? OR SCHEDUL? OR OCCASION? OR DAY? ? OR HOUR? ? OR
MINUT-
               E? ? OR SECOND? ? OR PERIOD? OR CHRONOLOG?
S4    1463812   SIMULTANEOUS? OR SYNCHRON? OR COINCID? OR COEXIST? OR
CONC-
               URR? OR COORDINAT? OR SAME(2N)TIME? ?
S5    1095852   S3:S4(7N)(SWITCH? OR IMPLEMENT? OR REGULAT? OR CONTROL?
OR
               SUBSTITUT? OR RELAY? OR REDIRECT? OR REVERS? OR SHIFT? OR
DIV-
               ERT? OR REROUT? OR SHUNT? OR ACTUAT? OR TRIGGER?)
S6    2271030   PIPE? ? OR WIRE? ? OR BUFFER? OR THREAD?
S7     158562   S6(7N)(SELECT? OR BASE? ? OR PICK??? OR CHOOSE? OR
DETERMI-
               N? OR CHOSEN OR IDENTIFY? OR IDENTIFIES OR SPECIF? OR
DESIGNA-
               T? OR INDICAT? OR DESIR???)
? s s1:s2 and s5 and s7
            3194  S1:S2
         1095852  S5
          158562  S7
      S8       4  S1:S2 AND S5 AND S7
? t 8/k/all
```

8/K/1 (Item 1 from file: 350)

DIALOG(R)File 350:(c) 2006 The Thomson Corporation. All rts. reserv.

...delay of memory by overloading specific delay path procedure to provide
path delay calculations for timing **of address,** control **and data bus signals of memory**

...The path delay of the memory is designed by overloading very high
speed integrated circuits **hardware description language** initiative
towards application specific integrated circuit libraries (VITAL) path delay procedures to provide path delay calculations for **timing** of address, **control** and data bus signals of memory.

Technology Focus

INDUSTRIAL STANDARDS - The syntax and format of the very high speed integrated circuits **hardware description language (VHDL)** conforms
to IEEE 1076 standard.

Original Publication Data by Authority

Original Abstracts:

...to determine timing constraint violations of the timing bus signals of
the memory. The VITAL **wire** delay procedures are overloaded to